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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,580	06/29/2000	Youfeng Wu	042390.P8653	9087

7590 08/27/2003

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EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,580	WU ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Information Disclosure as received on 11/02/00.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by "Exploiting Basic Block Value Locality with Block Reuse", Huang et al. (herein referred to as Huang).

5. Referring to claim 8 Huang has taught an apparatus comprising:

a buffer to hold reuse region instance information pertaining to a plurality of instances of a reuse region (Huang abstract lines 13-15); and

a processing core to predict a data output of the reuse region based on the reuse region instance information, and to speculatively execute instructions using the predicted data output of the reuse region (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

6. Referring to claim 9 Huang has taught wherein the processing core is configured to determine whether a data output of the reuse region is to be predicted (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

7. Referring to claim 10 Huang has taught wherein the processing core is further configured to search the buffer for a matching instance and to determine whether the reuse region is identified by a normal reuse instruction (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

8. Referring to claim 11 Huang has taught wherein the reuse region instance information includes input information and output information for each instance of the reuse region (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

9. Referring to claim 15 Huang has taught wherein the processing core is further configured to predict a current set of live-out registers of the reuse region, and to predict an output value for each live-out register within the current set of live-out registers using at least one prediction technique and a prediction list maintained in the buffer (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5, 13-14, 18-20, 22-23, 24-26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang.

11. Referring to claims 1, 18, and 24 Huang has taught a system for speculatively reusing regions of code, the system comprising:

a memory to store regions of code (Huang abstract lines 8-10, 13-15); and

a processor, coupled to the memory, identifying a reuse region and a data input to the reuse region (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2);

determining whether a data output of the reuse region is contained within reuse region instance information pertaining to a plurality of instances of the reuse region (Huang abstract, page 1 column 2 paragraphs 2 and 3, page 2 column 1).

Huang has not taught when the data output is not contained within the reuse region instance information, predicting the data output of the reuse region based on the reuse region instance information. However, one of ordinary skill in the art at the time of the invention would have recognized the benefit in both reusing blocks of code that have been previously executed and in predicting the actual data values that will be produced even before the instructions are executed (Huang page 1, column 2 paragraph 1). So even though not every input combination will be recorded for every reuse block of instructions in the block history buffer, one would see the benefit in predicting what the output would be for the present block if its input combination has not been executed before, to try and produce the answers faster than waiting for the processor to execute the instructions in the block. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to predict the data output of the reuse region even if

the exact details of the current instance are not stored in the block reuse buffer to speed up the completion of the program through the common practice of instruction speculation and prediction to allow the processor to continue processing new instructions before the older instructions would be complete.

12. Referring to claims 2 and 25 Huang has taught wherein determining whether the reuse region instance information contains a data output comprises:

determining whether the data input to the reuse region matches any input information within the reuse region instance information and when the data input matches input information within the plurality of instances, determining whether the reuse region is identified by a normal reuse instruction (Huang abstract, page 2 column 1).

13. Referring to claims 3, 20, and 26 Huang has taught wherein the reuse region instance information includes input information and output information for each instance of the reuse region (Huang abstract, page 2 column 1).

14. Referring to claims 5, 19, and 28 Huang has taught wherein predicting the data output further comprises:

predicting a current set of live-out registers of the reuse region (Huang abstract page 1 columns 1 and 2, page 2 column 1); and

predicting an output value for each live-out register within the current set of live-out registers using at least one prediction technique and a prediction list maintained in the buffer (Huang abstract page 1 columns 1 and 2, page 2 column 1).

15. Referring to claims 13 and 22 Huang has not taught wherein the buffer includes a prediction list having a plurality of pointers to reuse region instances held in the buffer, a pointer

to the most currently used instance being located on the top of the prediction list and a pointer to the least currently used instance being located at the bottom of the prediction list. (Huang abstract, pages 1 and 2; it is inherent that the buffer would have to be sorted in some manner to allow the system to search for particular entries for certain blocks of code). Official Notice is taken, that one of ordinary skill in the art at the time of the invention would have recognized that the buffer could be used as a list, which would use pointers to show the different entries in the list.

16. Referring to claims 14 and 23 Huang has not taught wherein the buffer includes a value prediction table having an entry that includes a predicted output value, the predicted output value being located using an index. Huang has taught where the indexing is done by the address of the first instruction in the instruction block (Huang page 3 column 2 paragraph 2). Since there appears to be no certain benefit of indexing using the output value over indexing using the instruction address of the first instruction in the block, it is simply a design choice, and is not necessarily patentable. One of ordinary skill in the art at the time of the invention would recognize that the buffer, or list, would have to be indexed by some means or value located in the list, and by choosing a value that is in the list, the system can find all the entries for a particular output value. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an index of some value in the list, including the output value of the block, and that using a particular value over another is a design choice.

17. Claims 4, 6-7, 12, 16-17, 21, 27, and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Kulkarni et al, U.S. Patent Number 5,742,805 (herein referred to as Kulkarni).

18. Referring to claims 4, 12, 21, and 27 Huang has not explicitly taught wherein the reuse region instance information further includes a plurality of confidence counters for each live-out register of the reuse region, each of the plurality of confidence counters being associated with a certain prediction technique. However, using a counter to show the accuracy of prediction is well known in the art. Kulkarni has taught using a confidence counter to show the accuracy in a prediction for an instruction (Kulkarni column 2 lines 39-47). Using a counter to show how accurate the prediction for an instruction, or a group of instructions, will allow the system to predict when the accuracy is high, and to not predict and just to continue to execute when the prediction accuracy is low. This will prevent the system from having many mispredictions, which are costly to the system in terms of time lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention would use an accuracy counter for predictions for instructions to prevent having some mispredictions which slow the system down, thus reducing the time for execution.

19. Referring to claims 6, 16, and 29 Huang has taught wherein predicting an output value for each live out register further comprises selecting the at least one prediction technique from multiple prediction techniques (Huang abstract page 1 columns 1 and 2, page 2 column 1; page 1 column 2 paragraph 1).

Huang has not explicitly taught wherein predicting an output value for each live out register further comprises selecting the at least one prediction technique from multiple prediction techniques based upon a plurality of confidence counters associated with the live-out register, each of the plurality of confidence counters corresponding to a certain prediction technique. However, using a counter to show the accuracy of prediction is well known in the art. Kulkarni

has taught using a confidence counter to show the accuracy in a prediction for an instruction (Kulkarni column 2 lines 39-47). Using a counter to show how accurate the prediction for an instruction, or a group of instructions, will allow the system to predict when the accuracy is high, and to not predict and just to continue to execute when the prediction accuracy is low. This will prevent the system from having many mispredictions, which are costly to the system in terms of time lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention would use an accuracy counter for predictions for instructions to prevent having some mispredictions which slow the system down, thus reducing the time for execution.

20. Referring to claims 7, 17, and 30 Huang has taught wherein multiple prediction techniques comprise a context-based prediction technique, a stride prediction technique, and a last value prediction technique (Huang page 1 column 2 paragraph 1).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Gonzalez et al, "Trace-Level Reuse", has taught reusing blocks of instructions be predicting the output of the block of instructions based on previous instances of the block.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

August 19, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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